Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

1 (Currently Amended). A field effect transistor with a dual-gate, comprising:

a monocrystalline conduction channel of a first width and a dual-gate of 100 mm or less,

source and drain regions located at opposite ends of said monocrystalline conduction channel, said source and drain regions having silicide sidewalls on a surface thereof wherein source-drain resistance is reduced, and

self-aligned polysilicon gate regions on opposing sides of said monocrystalline conduction channel and recessed from said source and drain regions wherein gate-junction capacitance is reduced, said polysilicon gate regions having silicide sidewalls formed thereon,

wherein the smallest feature of said field effect transistor formed through a lithographic process is of a second width, wherein said first width is smaller than said second width ~~and wherein said first width is defined as sub-lithographic~~.

2 (Original). A field effect transistor as recited in claim 1, wherein said silicide sidewalls are in the form of a liner.

3 (Currently Amended). A field effect transistor as recited in claim 1, wherein said polysilicon gate regions are connected by a connector.

4 (Original). A field effect transistor as recited in claim 3, wherein said connector is a damascene connector.

5 (Previously Presented). A field effect transistor as recited in claim 4, wherein said damascene connector is formed in a trench in at least one of an isolation structure or a pad material extending over an edge of said polysilicon gate regions.

6 (Original). A field effect transistor as recited in claim 1, wherein said silicide sidewalls are connected by a connector.

7 (Previously Presented) A field effect resistor transistor as recited in claim 6, wherein said connector is a Damascene damascene connector.

8 (Previously Presented). A field effect transistor as recited in claim 7, wherein said damascene conductor connector is formed in a trench in at least one of an isolation structure or a pad material extending over an edge of said polysilicon gate regions.

9 (Canceled).

10 (Canceled).

11 (Canceled).

12 (Canceled).

13 (Canceled).

14 (Canceled).

15 (Canceled).

16 (Canceled).

17 (Canceled).

18 (New). A field effect transistor as in claim 1, wherein said length of said conduction channel is at least two to four times said first width.

19 (New). A filed effect transistor as in claim 1, wherein said conduction channel has a width of approximately 5nm.

20 (New). A field effect transistor as recited in claim 1, further including an insulating material between said source and drain regions, respectively where said polysilicon is recessed.

21 (New). A field effect transistor as recited in claim 1, wherein said source and drain regions and said conduction channel are formed of monocrystalline silicon on an insulator, wherein said source and drain regions have a width greater than said conduction channel.

22 (New). A field effect transistor as recited in claim 20, wherein shallow trench isolation structure is formed by said insulating material.